Amendments to the Claims:

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)
10. (Cancelled)
11. (Cancelled)
12. (Original) A method of fabricating a semiconductor package, comprising the steps of:

a) providing a leadframe which includes:

a die paddle having opposed, generally planar top and bottom surfaces; and

a plurality of leads which extend at least partially about the die paddle and each have opposed, generally planar upper and lower lead surfaces and an inner lead end;

b) etching the leadframe such that each of the leads includes a half etched portion which is formed in the lower lead surface, extends to the inner lead end, and defines a generally planar etched lead surface which is disposed in opposed relation to the upper lead surface and extends in generally co-planar relation to the top surface of the die paddle;

c) attaching a semiconductor chip to the top surface of the die paddle;

d) electrically connecting the semiconductor chip to at least one of the leads; and

e) at least partially encapsulating the leadframe and the semiconductor chip with an encapsulation material such that at least a portion of the lower lead surface of each of the leads is exposed in the encapsulation material.

13. (Original) The method of Claim 12 wherein step (b) comprises etching the leadframe such that each of the leads has a lead thickness between the upper and lower lead surfaces thereof which exceeds a paddle thickness of the die paddle between the top and bottom surfaces thereof.

14. (Original) The method of Claim 13 wherein step (b) comprises etching the entirety of the top surface of the die paddle and etching a portion of the lower lead surface of each of the leads in amounts sufficient to cause the lead thickness of each of the leads to exceed the paddle thickness and the top surface of the die paddle to extend in generally co-planar relation to the etched lead surface of each of the leads.

15. (Original) The method of Claim 14 wherein the etching of the top surface of the die paddle and the etching of a portion of the lower lead surface of each of the leads to form the half etched portion therein is conducted simultaneously.

16. (Original) The method of Claim 12 wherein step (d) comprises electrically connecting the semiconductor chip to the upper lead surface of at least one of the leads via a conductive wire which is encapsulated by the encapsulation material.

17. (Original) The method of Claim 12 wherein step (e) comprises applying the encapsulation material such that the bottom surface of the die paddle is exposed therein.

18. (Original) The method of Claim 17 wherein step (a) comprises providing a leadframe wherein the bottom surface of the die paddle and the lower lead surface of each of the leads extend in generally co-planar relation to each other.

19. (Original) The method of Claim 17 further comprising the step of:

g) plating the bottom surface of the die paddle and the lower lead surface of each of the leads with a corrosion-minimizing material.

20. (Original) The method of Claim 12 wherein step (e) comprises applying the encapsulation material such that at least a portion of the upper lead surface of each of the leads is exposed therein.

21. (Original) The method of Claim 12 wherein step (a) further comprises plating the upper lead surface of at least one of the leads with an electrical conductivity enhancing material.

22. (Original) A method of fabricating a leadframe for use in a semiconductor package, comprising the steps of:

a) providing a die paddle having opposed, generally planar top and bottom surfaces, and a plurality of leads which extend at least partially about the die paddle and each have opposed, generally planar upper and lower lead surfaces and an inner end; and

b) etching the die paddle and the leads such that each of the leads includes a half etched portion which is formed in the lower lead surface, extends to the inner lead end, and defines a generally planar etched lead surface which is disposed in opposed relation to the upper lead surface and extends in generally co-planar relation to the top surface of the die paddle.

23. (Original) The method of Claim 22 wherein step (b) comprises etching the die paddle and the leads such that each of the leads has a lead thickness between the upper and lower lead surfaces thereof which exceeds a paddle thickness of the die paddle between the top and bottom surfaces thereof.

24. (Original) The method of Claim 23 wherein step (b) comprises etching the entirety of the top surface of the die paddle and etching a portion of the lower lead surface of each of the leads in amounts sufficient to cause the lead thickness of each of the leads to exceed the paddle thickness and the top surface of the die paddle to extend in generally co-planar relation to the etched lead surface of each of the leads.

25. (Original) The method of Claim 24 wherein the etching of the top surface of the die paddle and the etching of a portion of the lower lead surface of each of the leads to form the half etched portion therein is conducted simultaneously.

26. (Original) The method of Claim 22 further comprising the step of:

c) plating the bottom surface of the die paddle and the lower lead surface of each of the leads with a corrosion-minimizing material.

27. (Original) The method of Claim 22 further comprising the step of:

g) plating the upper lead surface of at least one of the leads with an electrical conductivity enhancing material.

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (New) A method of fabricating a semiconductor package, comprising the steps of:

a) providing a leadframe which includes:

a die paddle having opposed, generally planar top and bottom surfaces; and

at least one lead which is disposed in spaced relation to the die paddle and has opposed, generally planar upper and lower lead surfaces and an inner end;

b) etching the leadframe such that the lead includes a half etched portion which is formed in the lower lead surface, extends to the inner lead end, and defines a generally planar etched lead surface which is disposed in opposed relation to the upper lead surface and extends in generally co-planar relation to the top surface of the die paddle; and

c) electrically connecting a semiconductor chip to the lead.

33. (New) The method of Claim 32 wherein step (b) comprises etching the leadframe such that the lead has a lead thickness between the upper and lower lead surfaces thereof which exceeds a paddle thickness of the die paddle between the top and bottom surfaces thereof.

34. (New) The method of Claim 33 wherein step (b) comprises etching the entirety of the top surface of the die paddle and etching a portion of the lower lead surface of the lead in amounts sufficient to cause the lead thickness of the lead to exceed the paddle thickness and the top surface of the die paddle to extend in generally co-planar relation to the etched lead surface of the lead.

35. (New) The method of Claim 34 wherein the etching of the top surface of the die paddle and the etching of a portion of the lower lead surface of the lead to form the half etched portion therein is conducted simultaneously.